

FIG. 1
(PRIOR ART)

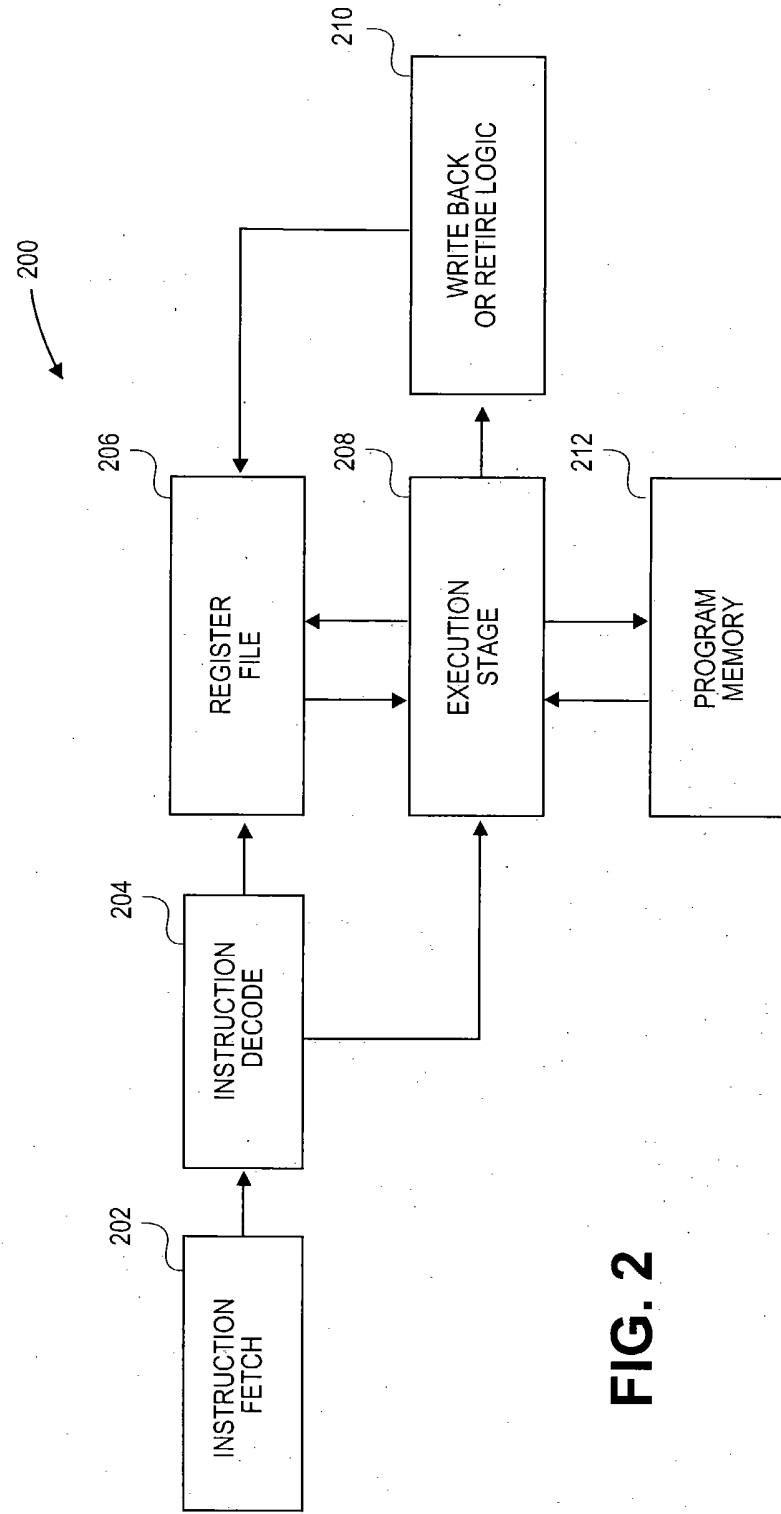


FIG. 2

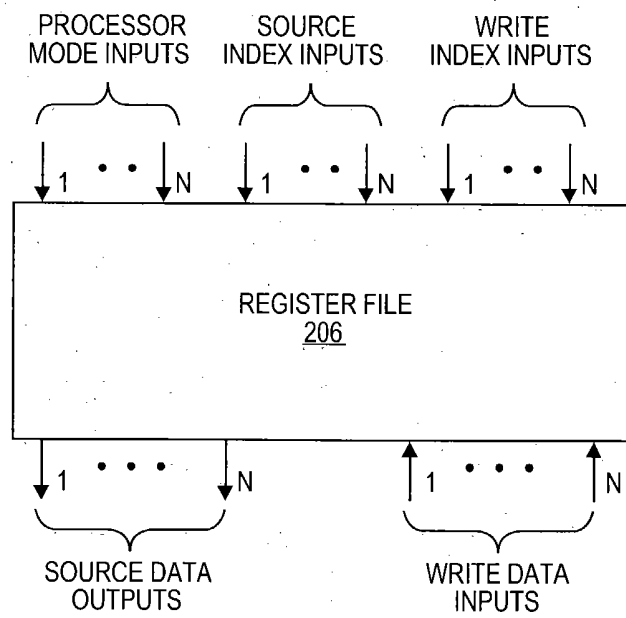


FIG. 3

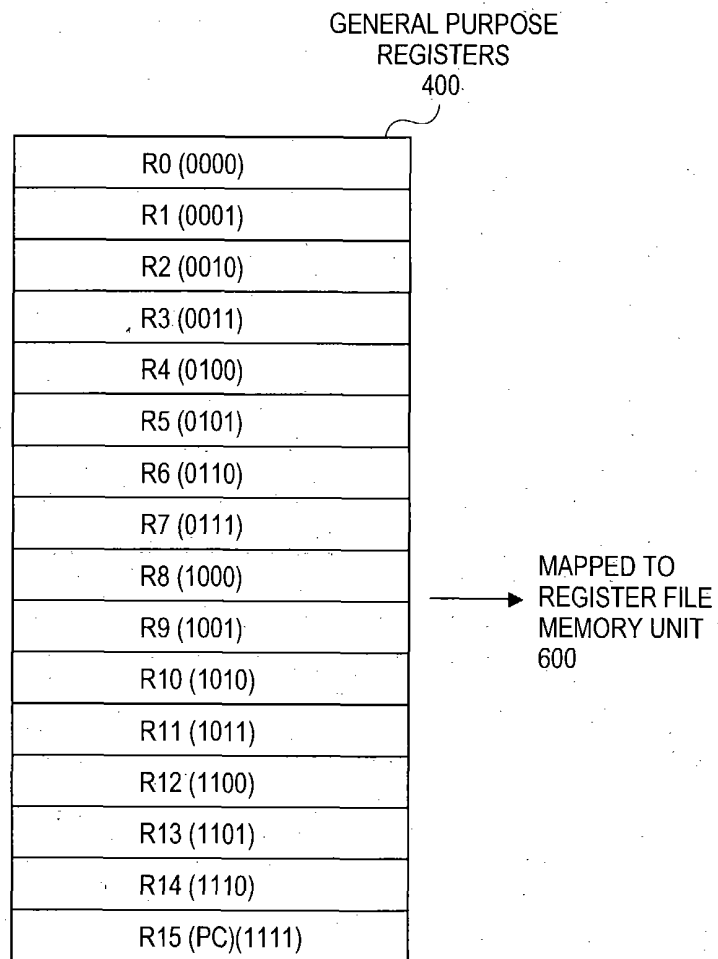


FIG. 4

Address	Processor Mode	Encoded Address
R0 (0000)	ALL	00000
R1 (0001)	ALL	00001
R2 (0010)	ALL	00010
R3 (0011)	ALL	00011
R4 (0100)	ALL	00100
R5 (0101)	ALL	00101
R6 (0110)	ALL	00110
R7 (0111)	ALL	00111
R8 (1000)	FIQ	01000
R9 (1001)	FIQ	01001
R10 (1010)	FIQ	01010
R11 (1011)	FIQ	01011
R12 (1100)	FIQ	01100
R13 (1101)	FIQ	01101
R14 (1110)	FIQ	01110
Reserved (1111)	ALL	01111
R14 (1110)	IRQ	10000
R13 (1100)	IRQ	10001
R14 (1110)	SVC	10010
R13 (1100)	SVC	10011
R14 (1110)	UND	10100
R13 (1100)	UND	10101
R14 (1110)	ABT	10110
R13 (1100)	ABT	10111
R8 (1000)	USR, UND, SVC, ABT, IRQ	11000
R9 (1001)	USR, UND, SVC, ABT, IRQ	11001
R10 (1010)	USR, UND, SVC, ABT, IRQ	11010
R11 (1011)	USR, UND, SVC, ABT, IRQ	11011
R12 (1100)	USR, UND, SVC, ABT, IRQ	11100
R13 (1101)	USR	11101
R14 (1110)	USR	11110
Reserved (1111)	ALL	11111

FIG. 5

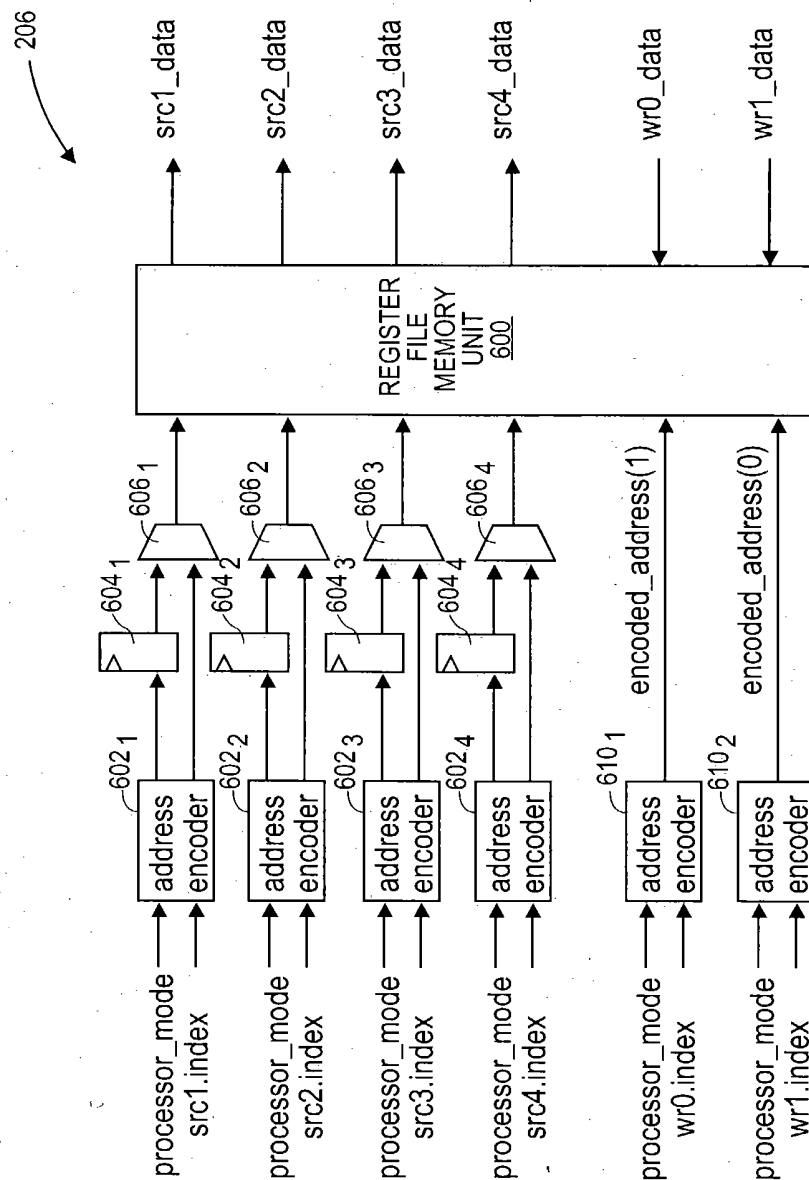


FIG. 6

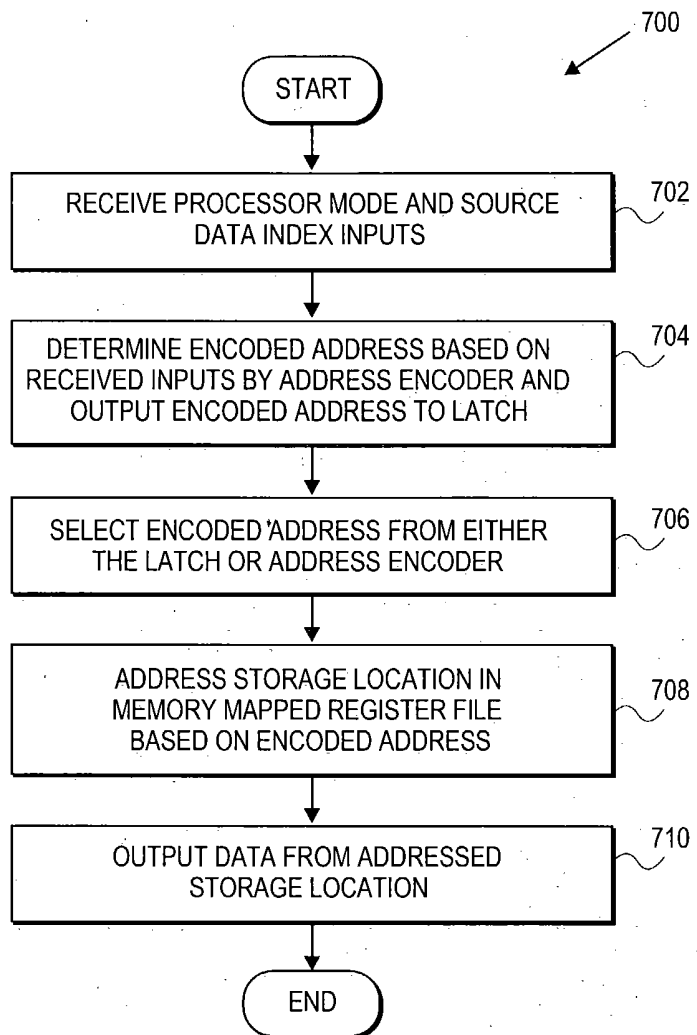


FIG. 7

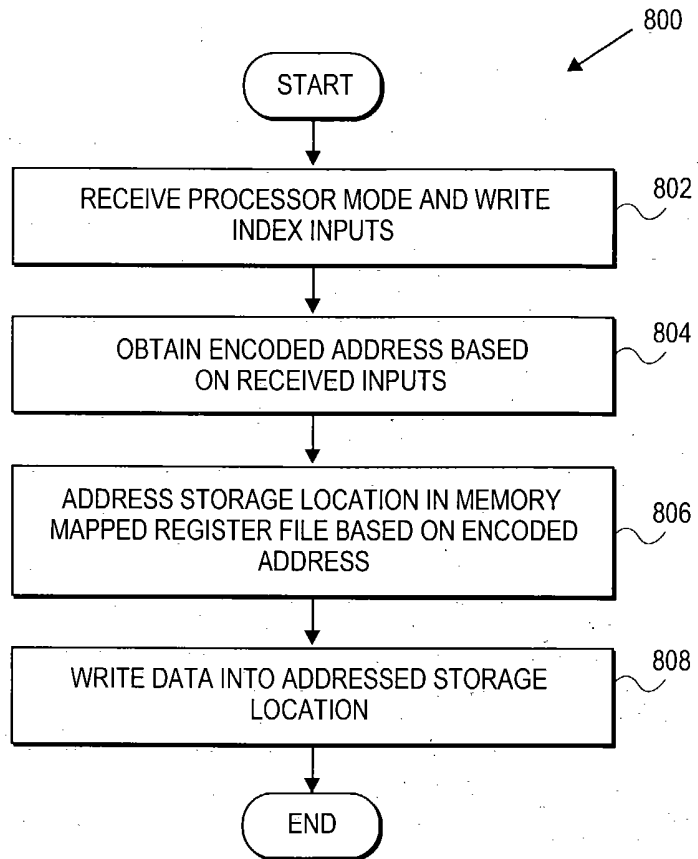


FIG. 8